Form PTO-1449 (Modified) Atty Docket No.: P18612 Serial No.: Unknown List of Patents and Publications Statement Applicant: Uday Shah et al. (Use several sheets if necessary) Filing Date: March 24, 2004 REFERENCE DESIGNATION **U.S. PATENT DOCUMENTS** Examiner Document No. Filing date Class Sub-Initials Class if appropriate AC AA 6,063,698 Tseng et al. 438 585 AB 6,184,072 B1 Kaushik et al. 438 197 AC 6,420,279 B1 Ono et al. 785 438 6,475,874 B2 AD Xiang et al. 438 396 Ahn et al. AE 6,514,828 B2 438 240 AF 6,544,906 B2 Rotondaro et al. 438 785 AĞ 6,617,209 B1 Chau et al. 438 240 AH 6,617,210 B1 Chau et al. 438 240 ΑI 6,620,713 B2 Arghavani et al. 438 585 AJ 6,689,675 B1 Parker et al. 438 585 AK 6,696,327 B1 Brask et al. 438 197 AL 6,696,345 B2 Chau et al. 438 387 AM US2002/0197790 A1 Kizilyalli et al. 438 240 US2003/0032303 A1 AN 770 Yu et al. 438 AC AO US2003/0045080 A1 Visokay et al. 438 591 **FOREIGN PATENT DOCUMENTS** Document No. Date Country Class Sub-Class Translation OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.) Polishchuk et al., "Dual Workfunction CMOS Gate Technology Based on Metal Interdiffusion". AC AQ www.eesc.berkeley.edu, 1 page Doug Barlage et al., "High-Frequency Response of 100nm Integrated CMOS Transistors with AR High-K Gate Dielectrics", 2001 IEEE, 4 pages Lu et al., "Dual-Metal Gate Technology for Deep-Submicron CMOS Devices", dated April 29, AS 2003, 1 page Schwantes et al., "Performance Improvement of Metal Gate CMOS Technologies with Gigabit AT Feature Sizes", Technical University of Hanburg-Harburg, 5 pages Doczy et al., "Integrating N-type and P-type Metal Gate Transistors," Serial No. 10/327,293, AU Filed December 20, 2002 Brask et al., "A Method for Making a Semiconductor Device Having a Metal Gate Electrode," ΑV Serial No. 10/704,497, Filed November 6, 2003 Brask et al., "A Method for Etching a Thin Metal Layer", Serial No. 10/704,498, Filed November AW Brask et al., "A Method for Making a Semiconductor Device with a Metal Gate Electrode that is AX Formed on an Annealed High-K Gate Dielectric Layer", Serial No. 10/742,678, Filed 12/19/03 Brask et al., "A Method for Making a Semiconductor Device that Includes a Metal Gate AY Electrode", Serial No. 10/739,173, filed December 18, 2003 Brask et al., "A CMOS Device With Metal and Silicide Gate Electrodes and a Method for Making It", Serial No. 10/748,559, filed December 29, 2003 Doczy et al., "A Method for Making a Semiconductor Device that Includes a Metal Gate BA Electrode", Serial No. 10/748,545, filed December 29, 2003 Examiner **Date Considered** Adoms 1106 EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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